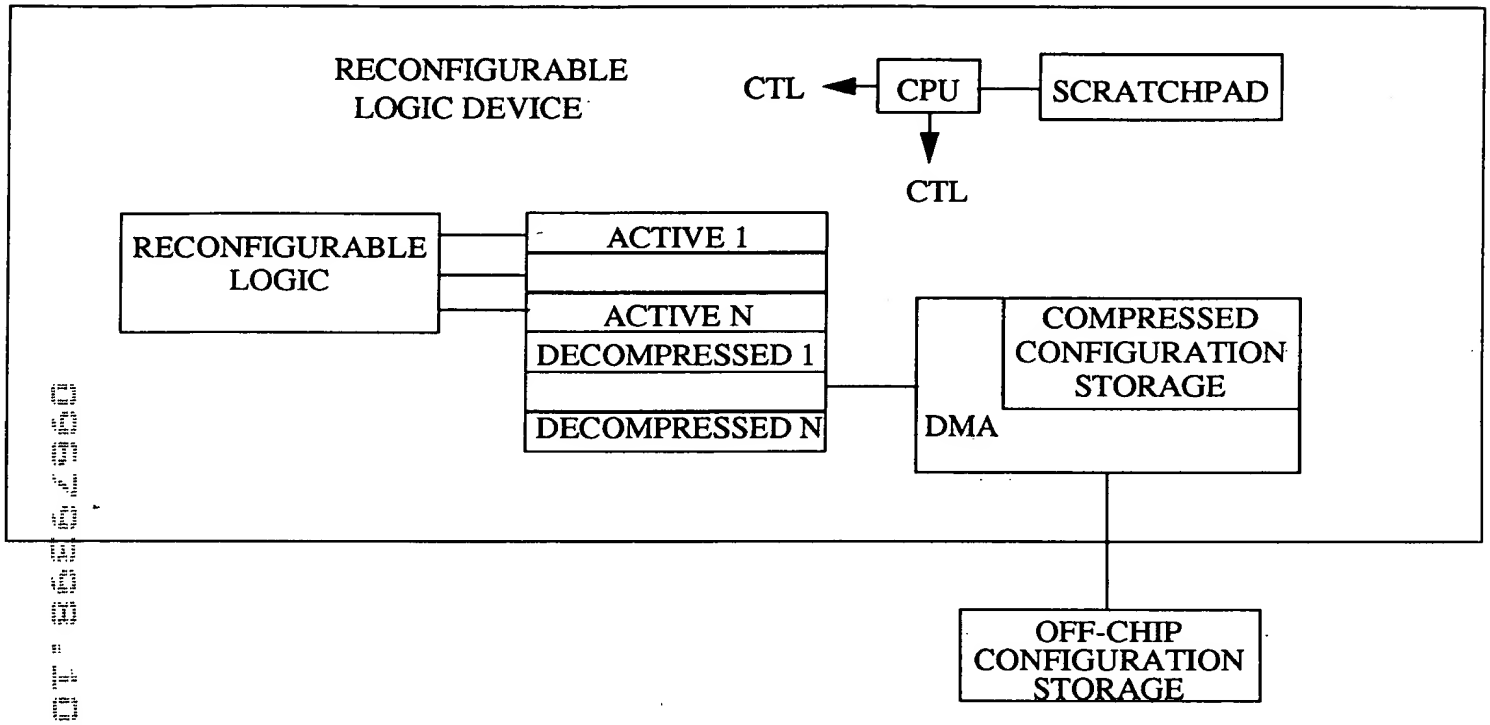
RECONFIGURABLE
LOGIC DEVICE
CTL
CPU
SCRATCHPAD
CTL
RECONFIGURABLE
LOGIC
ACTIVE 1
ACTIVE N
DECOMPRESSED 1
DECOMPRESSED N
COMPRESSED
CONFIGURATION
STORAGE
DMA
OFF-CHIP
CONFIGURATION
STORAGE

Fig. 1

Y:	X: 0	1	2
2	1	1	9
1	7	7	7
0	1	3	9

Fig. 2a

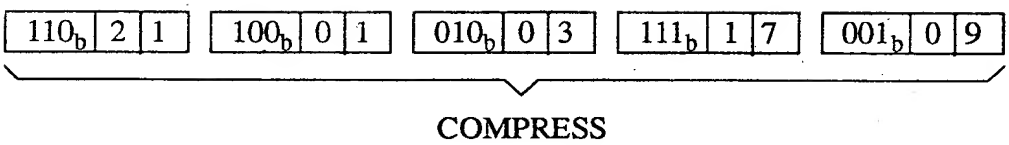

Fig. 2b

08808054 "86808 2 98

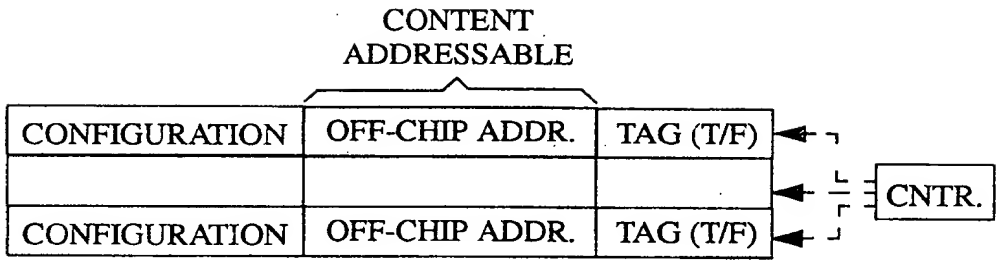

Fig. 3

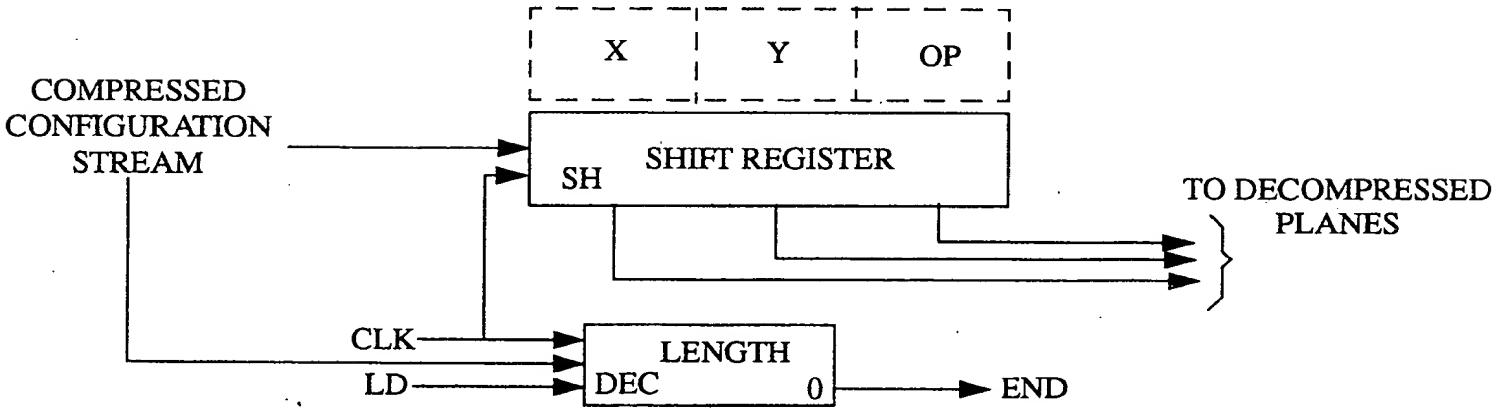

Fig. 4

SCRATCHPAD

PLANE	CONFIG. ADDR.
0	A_0
1	A_1
N	A_N

Fig. 5

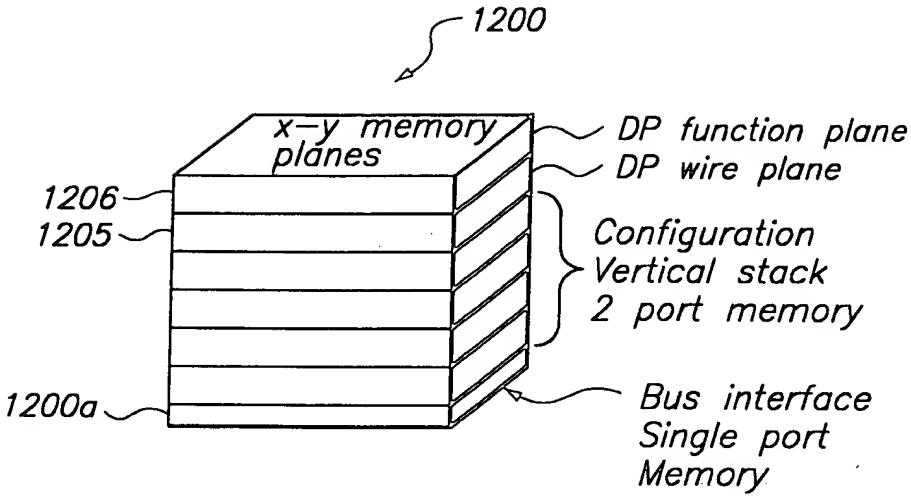
1200
x–y memory planes
DP function plane
DP wire plane
1206
1205
Configuration Vertical stack 2 port memory
1200a
Bus interface Single port Memory

FIG. 6a

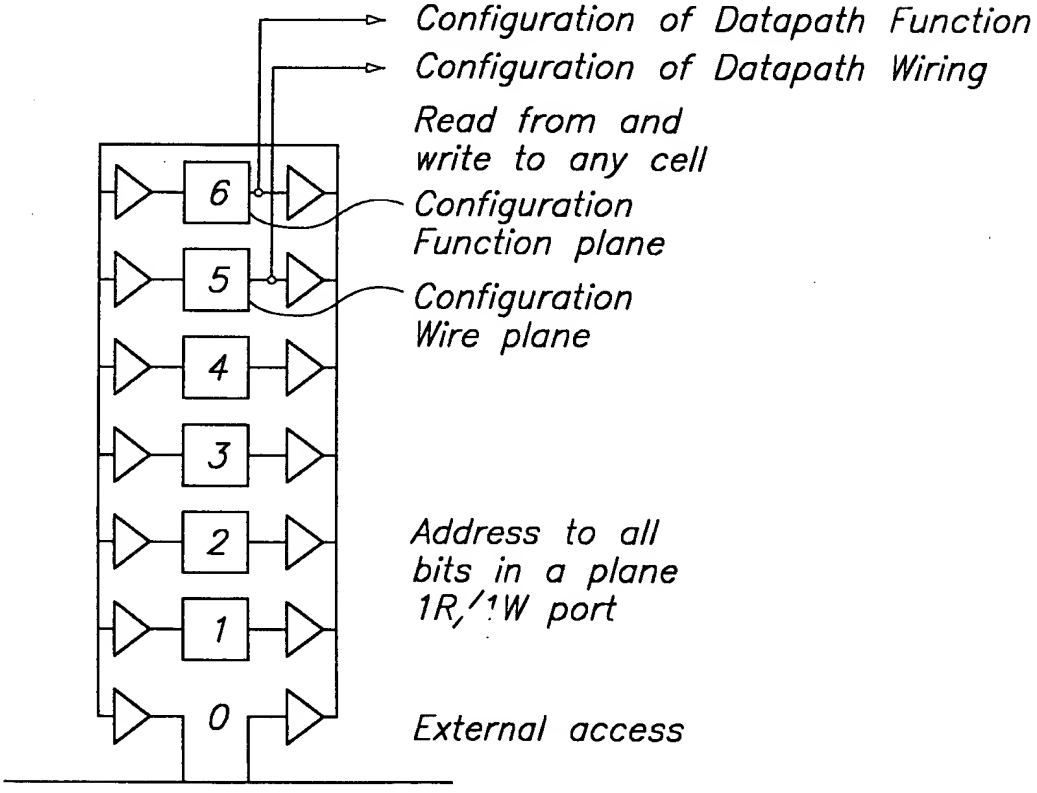
Configuration of Datapath Function
Configuration of Datapath Wiring
Read from and write to any cell
6
5
4
3
2
1
0
Configuration Function plane
Configuration Wire plane
Address to all bits in a plane 1R/1W port
External access

FIG. 6b

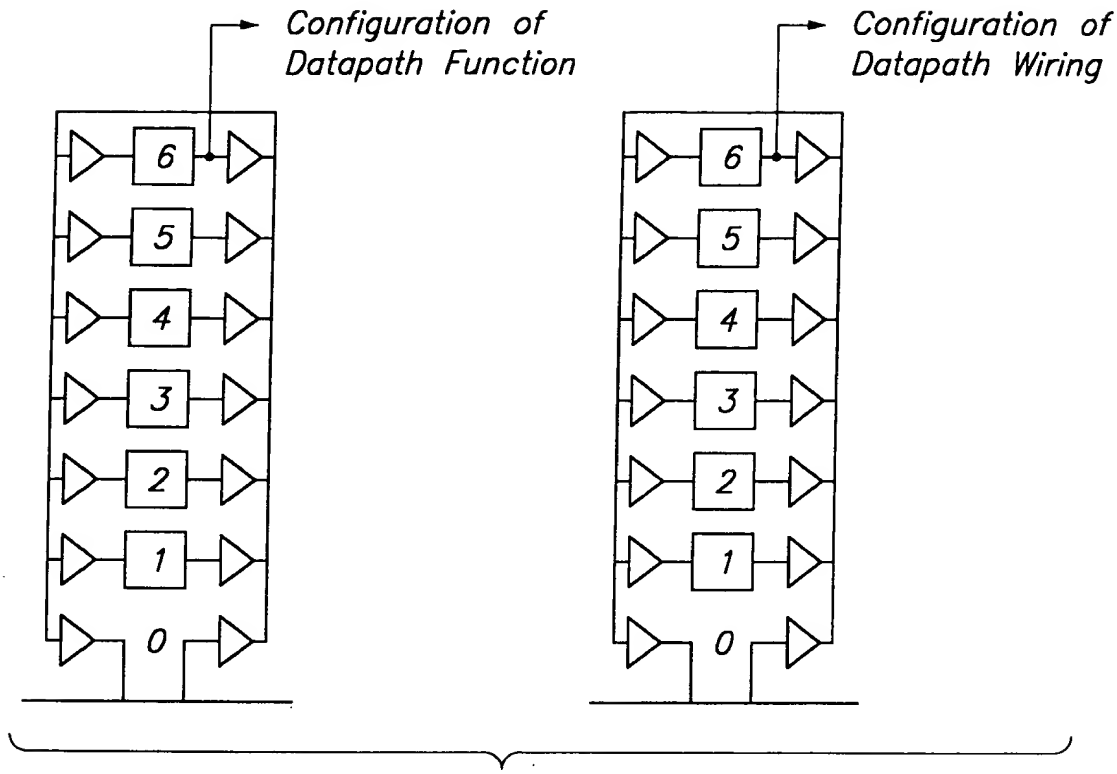
Configuration of
Datapath Function
Configuration of
Datapath Wiring
6
5
4
3
2
1
0
6
5
4
3
2
1
0

FIG. 6c

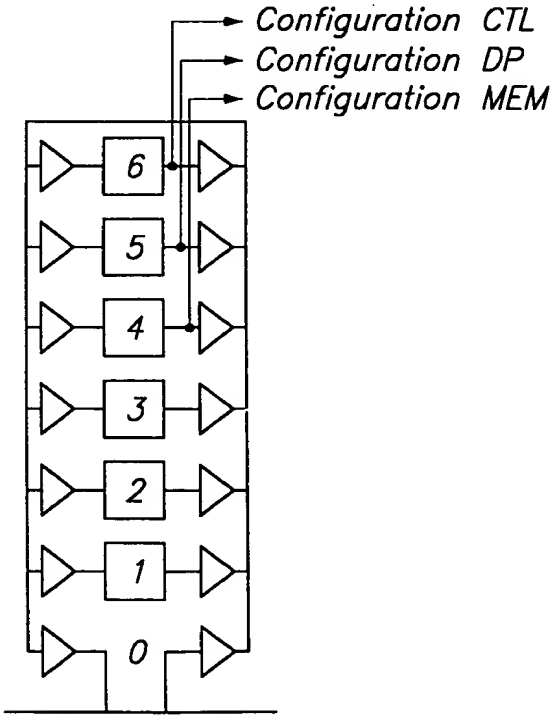
Configuration CTL
Configuration DP
Configuration MEM
6
5
4
3
2
1
0

FIG. 6d

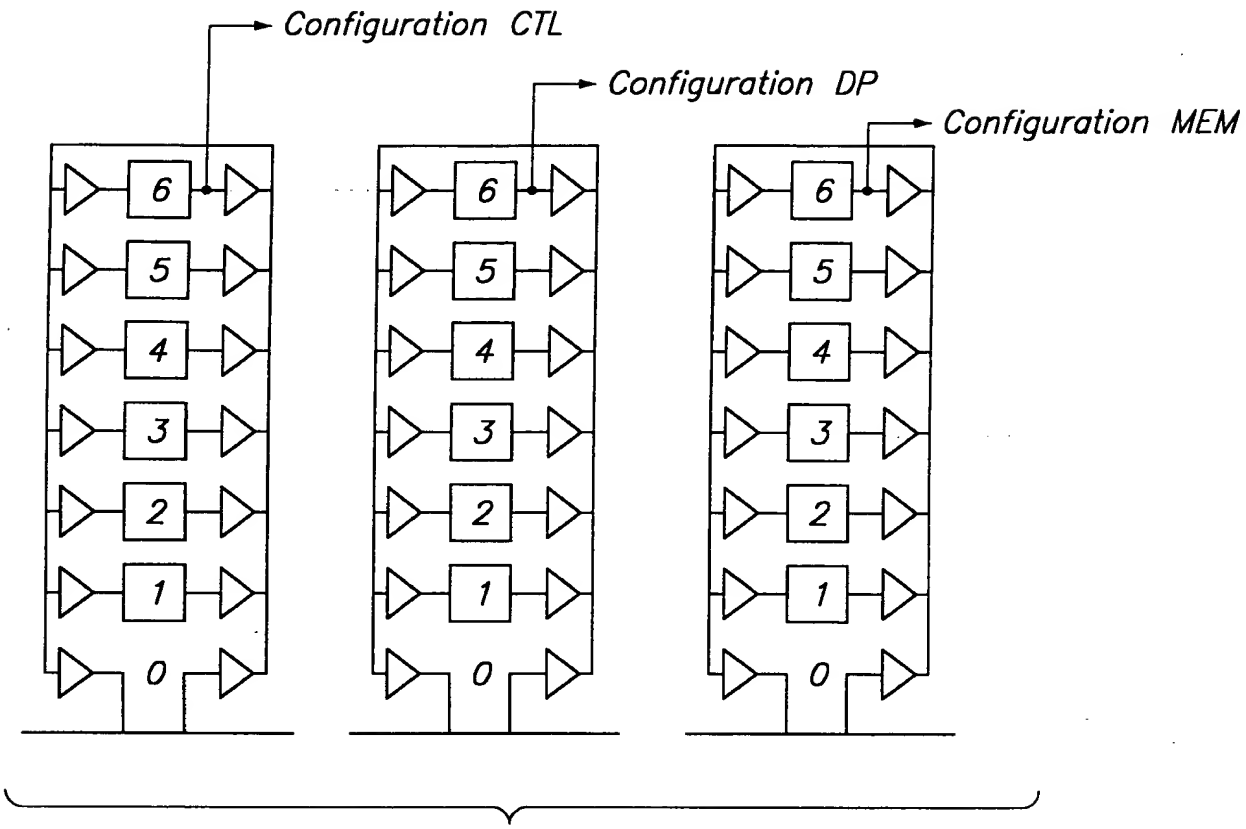
Configuration CTL
Configuration DP
Configuration MEM
6
5
4
3
2
1
0

FIG. 6e

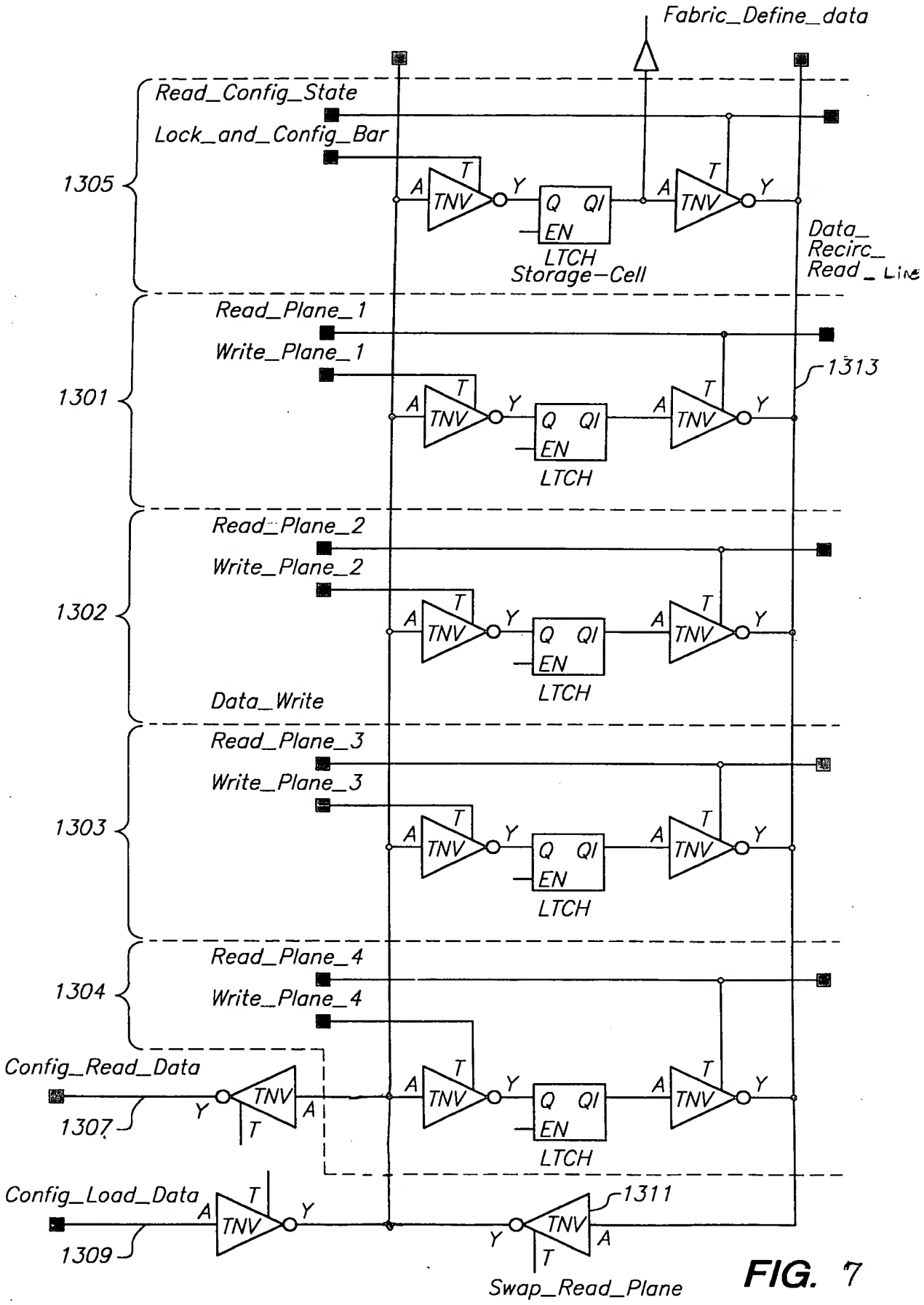
Fabric_Define_data
Read_Config_State
Lock_and_Config_Bar
1305
T
A
TNV
Y
Q QI
EN
LTCH
Storage-Cell
Data_
Recirc_
Read_Line
Read_Plane_1
Write_Plane_1
1301
1313
Read_Plane_2
Write_Plane_2
1302
Data_Write
Read_Plane_3
Write_Plane_3
1303
Read_Plane_4
Write_Plane_4
1304
Config_Read_Data
1307
Config_Load_Data
1309
1311
Swap_Read_Plane

FIG. 7